

Curriculum Vitae

Vason P. Srini
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Fields of Specialization

High End Computing (HEC) system design for real-time processing, simulation, and visualization. VLSI implementation and FPGA based verification using Spatial Direct-Mapped (SDM) design methodology for low-power and low-weight. Application domains: autonomous vehicles (AGVs and UAVs), radar applications (digital array radar frontend, LADAR/Lidar), image processing applications (3D image processing and 3D image construction, hyperspectral imaging), network applications, life science applications (protein folding), and multimedia applications.

Architecture design, simulation, and implementation using reconfigurable parallel vector and stream processors and MIMD model of computation.

Library compiler design and optimizations for the above architectures and domains using languages such as Fortran90/95, Matlab, Java, and Cg.

System on a chip (SOC) design and implementation using a four level (system, architecture, component, and physical) methodology for the direct mapping of an application to multiple processors on a chip. (Matlab, Simulink or a block diagram like specification to silicon)

VLSI system design and implementation using Cadence, Mentor, and Synopsys tools.

Distributed real-time system (DRTS) design and implementation using formal methods and Java.

Areas of Current Research

High end computing (HEC) systems (hardware and compiler) research using platform FPGAs, DDR memory components, hundreds of SerDes, lasers, detectors, and modulators for signal processing applications, life science applications, and environment modeling and monitoring applications.

Portable multimedia terminal design with high data rate wireless access for use in rural areas and global connectivity using many times and many where wireless networks. (Rural e-commerce is the application for these terminals)

Parallel vector processing and stream processing based DSP architecture design, simulation, and implementation for use in 3D cellphones and smart mobile devices.

Research in system on a chip containing processors, smart memory, wireless

communication (RF), data converters, and multimedia support with emphasis on low-power, parallel stream data processing, wideband architecture for transceivers, image processing, and reconfiguration.

Recent Research Talks

Konkuk Univ., CS Dept., Seoul, Korea. Workshop. June 13, 2005, Parallel and Distributed Real-time System (DRTS) Design for Autonomous Guided Vehicles (AGVs).

HyperComp Inc., Malibu, CA, Seminar, May 26, 2005, Scalable Computing Fabric for High end computing.

KAIST, Robotics Group, Daejong, Korea, Seminar, May 19, 2005, Grand Challenges for computer Science – DARPA Grandchallenge Robotics Race 2005.

Yonsei Univ., CS Dept. Seoul, Korea, Seminar, April 29, 2005, Telescoping Languages Approach to Compilers for Scalable Computing Fabric.

Konkuk Univ., CS Dept. Seminar, April 21, 2005, Grand Challenges for CS.

UCI Workshop, Jeju, Korea, March 30, 2005, Universal Telecommunication Oriented Personal Information Access (UTOPIA) - An Intl. IT Collaboration Project Proposal.

Yonsei Univ., Wonju Campus, Korea, Computer Engineering Dept. Seminar, March 24, 2005, Smart Devices for Rural E-commerce.

E-biz 2000 International Conference, Seoul, Korea – March 23, 2005, Rural E-commerce: Challenges and Opportunities.

Yonsei Univ., Processor Research Group, Seminar, Feb. 18, 2005, Parallel Embedded System Design Technology.

Nean 2005 Intl. Conference, Seoul, Feb. 5, 2005, Regional Co-operation in NEA for Enabling UTOPIA.

IIT Bombay, Dec. 27, 2004, Grand Challenges for CS – DARPA AGV Race.

Yonsei Univ., Nov. 3, 2004, Stream Processing for Video, Graphics, and Imaging Systems.

Samsung, Telecommunications and Networks Div., SOC Seminar, Suwon, Kiorea, Oct. 28, 2004, Rapid Design of SoC and SoP.

Yonsei Univ., 3D Graphics Group, Seminar, Sept. 22, 2004, Parallel Embeddable System Design Technology.

National/International Involvement

Participated in the National HECRTF (High end computing revitalization task force) workshop in June 2003 to help set the direction for future HEC.

Teaching Experience - Graduate Level Courses

Parallel Embedded Computer Architecture – design, analysis, and implementation

Advanced computer systems architecture - two course sequence

Compiler optimizations for parallel architectures and scalable computing fabric (SCF)

VLSI design, implementation, chip testing, and system integration - three course sequence

Parallel models of computation and programming parallel systems - two course sequence

Computer networks design, analysis, and simulation - two course sequence

Computer Aided Design of VLSI systems - two course sequence

Operating system design, implementing parts of an OS, and performance analysis

Digital systems design, simulation, and implementation using FPGAs - two course sequence

Teaching Experience - Undergraduate Level Courses

Design and analysis of digital circuits

AI Techniques

Programming languages and data structures

Analysis and design of algorithms

Formal languages and automata

Computer operating system principles

Compiler construction

Introductory courses in digital systems, programming, networks, digital communication, assembly language programming, and discrete mathematics

Skill development courses

X86 architecture, programming, and interface design; Unix device driver design and implementation; GPSS simulation; Unix systems programming; VHDL modeling and simulation; VLSI tools from UCB, Mentor, Cadence, and Synopsys

Education

Ph.D. Computer Science - Major: Computer Architecture, Minor: Operating Systems, University of Louisiana, Lafayette, LA 70504. (1980)

M.S. Electrical Engineering - Digital Systems, Tennessee Technological University, Cookeville, TN 38501. (1971)

B.E. Electrical Engineering - Computer Design, University of Madras, College of Engineering, Guindy, Madras 600025. (1969)

Editorial and other Activities

Editor of IEEE Transactions on Computers 1990-94.

Referee for many conferences and journals.

Member of Computer Science Accreditation Board (CSAB).

Professional Background

Present: Professor of Computer Science (Visiting), Yonsei University, Seoul, Korea and Executive Director at Data Flux Systems Inc., Berkeley, CA working on "High End Computer Architectures" for 3D Graphics and image processing; solving grand challenge problems in scientific simulation, drug discovery, environment monitoring, and global surveillance using satellites; helping the UC Berkeley's Berkeley Wireless Research Center (BWRC) in BEE2 supercomputer design based on platform FPGAs; and helping UC Irvin's DREAM Lab. in real-time sensor network architecture and navigation. sensor processing for autonomous ground vehicle (AGV). Team leader for developing Navigation sensor processing software for the Cyberrider AGV participating in the DARPA Grandchallenge Race (www.cyberrider.org).

June 2001 to August 16, 2002: Technical Director, Ellipsis Digital Systems Inc., Carlsbad, CA. Chief hardware architect for VLSI chip embeddable realization of IEEE 802.11a/g standard using a component based methodology and Simulink/PtolemyII for analysis and simulation. Research Affiliate at Berkeley Wireless Research Center (BWRC), EECS Dept., UC Berkeley working on "Chip in a Day" design flow for baseband processing of wireless systems.

1991 to May 2001: Research and Development Director, Data Flux Systems Inc. and Research Affiliate with UC Berkeley's EECS Dept., working on innovative architectures for multimedia and wireless communication. Developed a MIMD parallel stream data processing system on a chip with 96 processors for communication, HDTV, and image processing applications. A prototype board with 48 processors has been completed and demonstrated at DAC 1998. EDA tools used: Cadence's CDS99A, Synposys' DC, MC and BC, Racal-Redac's Visula for PCB. Associated with UCB's Infopad, Berkeley Multimedia Research Center, and Berkeley Wireless Research Center (BWRC) from their inception.

Aug. 1999 to Sept. 2000: Applications Engineering Consultant, Mentor Graphics, San Jose, CA. Developed deep submicron flows for designing network systems to support data and voice communication, parallel processing systems on a chip, integrated analog frontend chips for DSL and cable modems, and voice over IP systems on a chip. Tools: ICStation, Calibre, xCalibre, Seamless, MachTA, Eldo, and Modelsim. Helped companies design systems using the tools, tapeout, and analysis. Worked on developing design flows for designing and implementing communication and processor chips in deep submicron technologies using ECAD tools from multiple vendors (Cadence, Synposys, and Mentor).

Oct. 1990 to 1994: Directed projects on wireless network simulation system tools, parallel visualization, concurrent engineering CAD, MCM design methodology for multitechnology fabrication, and parallel image processing for helicopters.

Sept. 1983 to Oct. 1990: Research Computer Science Professor - Computer Science Division, Univ. of California, Berkeley. Research Director of the DARPA funded AQUARIUS project to investigate parallel computer architecture research for numeric/symbolic computing with emphasis on logic programming (Prolog). VLSI design and implementation of high performance Prolog machines, crossbars (16 X 32 and 32 X 32), and cache memory. Research in silicon compilers (MacPitts), and operating system design for reconfigurable computer systems.

September 1980 to Aug. 1983: Associate Professor of Computer Science at the University of Alabama in Birmingham. Research in dataflow architectures, dynamically reconfigurable computer systems, and distributed operating systems. Teaching graduate level courses in computer architecture, VLSI, networks, and operating systems.

September 1979 to August 1980: Project Co-Director and Co-Principal Investigator with Dr. B.D. Shriver for Distributed Operating Systems and Architecture Research (Funded by Texas Instruments, Inc., Dallas, TX 75235, Corporate Engineering Center), USL, Lafayette, LA 70504.

September 1977 to June 1978: Assistant Professor of Computer Science, Tennessee Tech. University, Cookeville, TN 38501. Teaching senior and graduate courses in programming language systems, compiler construction, operating systems, and microcomputer system software. Research in language design and implementation, fault tolerance of microprocessor systems, and system design using multivalued logic.

June 1976 to August 1977: Lecturer in Computer Science Dept. VPI&SU, Blacksburg, VA 24061. Teaching senior and graduate level courses on advanced computing (VS2, JCL, data management, file management, access methods, and utility programs), simulation, and programming languages. Research in language design and implementation, fault diagnosis and fault tolerance of microprocessor systems.

November 1973 to June 1975: Senior Engineer at NCR Corp., Advanced Research & Development, Cambridge, Ohio, and Microprocessor Dept., Columbia, S.C. Corporate responsibility for independent investigation, design, and implementation of fault detection and location schemes in microprocessors and RAM's. Modeling memory and reliability analysis. Design of supervisor software for microprocessors.

September 1971 to June 1973: Graduate Asst. in EE Dept., VPI&SU, Blacksburg, VA 24061. Team member in the Software Development Group for GE 4020, IBM 370/155 network linkup. Research in computer understanding of speech, context sensitive parsing, and probabilistic automata.

August 1969 to August 1970: Electronics Engineer, Larsen & Toubro Ltd., Bombay. Developed digital circuits for Numerically Controlled Machines.

Summer Experience

1979 - Member of Technical Staff at Texas Instruments, Inc., Corporate Engineering Center, Dallas TX 75230. Developed interconnection structures for multiple processor systems. Developed highlevel approaches for interprocess communication using abstract dataflow protocol. Initiated research in distributed operating systems. Worked with corporate VLSI, and systems architecture groups.

1972 and 1973 - Systems Analyst at Isotope Geology Lab., VPI&SU, Blacksburg, VA 24061. Automating mass spectrometers using PDP 11/20 minicomputer.

1971 - Research Associate at Tennessee Tech. Univ., Cookeville, TN 38501. Responsible for building a 100 mW He Ne Laser and optical radar (LADAR). Conducted experiments in detecting the profiles of Fighter Aircraft using LADAR.

1968 and 1969 - Res. Asst. at Fundamental Engineering Research Establishment, College of Engineering, Guindy, Madras-25. Designed switching circuits and developed programs for IBM 1620.

Language and OS Experience

Languages: Java, C, VHDL, Prolog, C++, and Fortran77/90.

OS: Unix (BSD), Solaris, and Windows NT.

Patents

A patent on Crossbar for multiprocessors, 1991.

Recently Published Papers

Efficient Volume Visualization on GPU Clusters Using a Combination of Hierarchical Data Structures, Won-Jong Lee, Vason P. Srin, Tack-Don Han, Visualization Conference, Utah, Oct. 2005.

Adaptive and Scalable Load Balancing Scheme for Sort-Last Parallel Volume Rendering on GPU Clusters, Won-Jong Lee, Vason P. Srin, Tack-Don Han, Volume Graphics 2005 workshop, Stony Brook, NY, June 20, 2005.

Publications- Books and Journals

Aquarius-II Multiprocessor System Design and Simulation, Journal of Systems Integration, August 1997 (V.P.Srin, T.M.Nguyen, D.R.Busing, M.J.Carlton, G.E.Smine, B.K.Holmer, and A.M.Despain are the authors).

Defense Net: Technical Challenges in Command, Control, Communication, Computer, and Software (C4S) - Computer Society of India, Journal of Computer Science and Informatics, Vol. 23, No. 2, June 1993, pp 1 -26.

A Coprocessor System for Prolog, Hardware Accelerators, Adam Hilger Press, A.P. Ambler, P. Agrawal, and W. Moore, Ed., June 1988, UK. (V.P.Srini, J.V.Tam, T.M.Nguyen, B.K.Holmer, Y.N.Patt, and A.M.Despain are the authors).

A VLSI Processor for Prolog, Advanced Research in VLSI, P. Losleben Ed., 1987 Stanford VLSI Conference, MIT Press, Cambridge, MA (V.P.Srini, J.Tam, T.Nguyen, C.Chen, A. Wei, C.Chen, Y.N.Patt, and A.M.Despain are the authors).

An Architectural Comparison of Dataflow Systems, Computer Magazine, March 1986 pp 68 - 88.

A Fault Tolerant Dataflow System, Computer Magazine, March 1985.

A Methodology for Designing and Modeling Reconfigurable Systems, The Intl. Journal of Computer and Information Sciences, Oct. 1984 (V.P.Srini, and B.D.Shriver are the authors).

Dataflow, Encyclopedia of Computer Science and Engineering, A. Ralston Ed., Van Nostrand Reinhold Co., New York, 1983, pp 471 - 474.

Iterative Realization of Multivalued Logic Systems, IEEE Transactions on Computers (TC), Vol. C-28 No. 4, April, 1979, pp. 306-310.

Fault Location in a Semiconductor Random Access Memory Unit, IEEE TC, Vol. C-27 No. 4, April, 1978, pp. 349-358.

API Tests for RAM Chips, Computer Magazine, June, 1977, pp. 32-36.

Fault Diagnosis of Microprocessor Systems, Computer Magazine, January, 1977, pp. 60-65.

Realization of Fuzzy Forms, IEEE TC, Vol. C-24 No. 9, September, 1975, pp. 942-943.

Publications- Refereed Conference Papers

Reconfigurable HEC Platform , HECRTF Workshop, Washington DC, June 2003. (R. W. Brodersen, J. Wawrzynek, V. P. Srini, A. Vladimirescu, D. Orofino, J. Hwang, C. Chang, B. Richards, K. Camera, H. So, N. Zhou are the authors)

Reconfigurable Clusters of Memory and Processors Architecture for Stream Processing Systems, Intl. Conference on High Performance Computing, Bangalore, India, Dec. 2002 (V.P. Srini and J.M.Rabaey are the authors)

Reconfigurable Memory Module in the RAMP System for Stream Processing, Memory Workshop, Intl. Symposium On Computer Architecture (ISCA), Gothenberg, Sweden, July 2001. (V.P. Srini, J. Thendean, and J.M.Rabaey are the authors)

A Parallel DSP with Memory and I/O Processors, SPIE Conference, San Diego, CA, July 1998, Conf. 3452. (V.P. Srini, J. Thendean, S. Ueng, and J.M.Rabaey are the authors)

A Multiprocessor DSP System Using PADDI-2, Proceedings of the 35th Design Automation Conference (DAC), San Francisco, CA, June 1998. (V.P. Srini, R.A.Sutton, and J.M.Rabaey are the authors)

An Architecture for Web-based Image Processing, SPIE Conference, San Diego, CA, July 1997, Conf. 3166.

DFS - SuperMPX, A Parallel Processor for Image Processing, Intl. Conf. on Parallel Processing, St. Petersburg, Russia, Sept. 1995.

Parallel Volume Rendering of CFD Data on Massively Parallel Computers, Proceedings of the Symposium on CFD Applications on Parallel Processors, March 1993 (P. Sundaram, A. Rajkumar, and V. P. Srini are the authors).

The Aquarius IIU System. Proceedings of the First Intl. Conference on Systems Integration, Morristown, New Jersey, April 1990. (Darren R. Busing, Vason P. Srini, Georges E. Smine, Mike J. Carlton, and Alvin M. Despain are the authors)

Systems Integration of the VLSI-PLM Chip, Proceedings of the First Intl. Conference on Systems Integration, Morristown, New Jersey, April 1990. (Linda G. Bushnell, Vason P. Srini, and Lau T. Nguyen are the authors)

A Low-Latency Crossbar Chip for Multiprocessors, Proceedings of the 3rd International Symposium on VLSI Design, Bangalore, India, Jan. 1990, pp 33-52.

Crossbar-Multi-Processor (CMP) Architecture, Proceedings of the Workshop on Computer Architecture, Eilat, Israel, May 1989.

A Two-Tier Memory Architecture for High-Performance Multiprocessor Systems, Proceedings of the 1988 Supercomputing Conf., St. Malo, France, July 1988, pp 326 - 336. (T.M.Nguyen, V.P.Srini, and A.M.Despain are the authors).

A CMOS Chip for Prolog, Proceedings of the Intl. Conf. on Computer Design, Rye Town, New York, Oct. 1987, pp 605-610. (V.P.Srini, J.Tam, T.Nguyen, C.Chen, A. Wei, C.Chen, Y.N.Patt, and A.M.Despain are the authors).

Aquarius, Computer architecture News, March 1987 (A.M.Despain, Y.N.Patt, V.P.Srini, P.Bitars, W.Bush, C.Chien, W.Citrin, B.Fagin, W.Hwu, S.Melvin, R.Mcgeer, A.Singhal, M.Shebanow, and P.Van Roy are the authors).

Compiling Prolog Into Microcode: A case Study Using the NCR/32-000, Proceedings of the MICRO18 Conference, Asilomar, CA, Dec., 1985 (B.S.Fagin, Y.N.Patt, V.P.Srini, and A.M.Despain are the authors).

An Architecture for Concurrent Systems Research, Proceedings of the National Computer Conference, Chicago, July, 1985.

A Testbed for Numeric/symbolic Computing, Proceedings of the National Conf. on Computers, Hyderabad, India, Dec. 1984.

A Microprocessor with a Large Cache, Proceedings of the Intl. Conf. on Computers, Systems, and Signal Processing, Bangalore, India, Dec. 1984.

A Message-based Processor for Dataflow Systems, Proceedings of the 1984 Intl. Workshop on High-level Computer Architecture, Los Angeles, May 1984.

Node Reassignment in a Dataflow System, Proceedings of the 4th Intl. Conf. on Distributed Computing, San Francisco, May 1984.

IPC in UNIX using a restricted TCP/IP, Proceedings of the Intl. Conf. on Communications, Amsterdam, May 1984 (V.P.Srini, and R.N.Murphy are the authors).

Issues in reconfigurable operating system design, Proceedings of the 17th Hawaii Intl. Conf. on System Sciences, Hawaii, Jan. 1984.

An Architectural Comparison of two MIPS (NCR 32000 and SU-MIPS), Proceedings of the Wescon '83, San Francisco, Nov. 1983.

Test Generation from MacPitts Designs, Proceedings of the Intl. Conference on Computer Design (ICCD), New York, Oct. 1983.

Analysis of Cray-1S architecture, Proceedings of the 10th Intl. Symposium on Computer Architecture, Stockholm, Sweden, June 1983 (V.P.Srini, and J.F.Asenjo are the authors).

Performance Analysis of Cray-1S using Dataflow Graphs, Proceedings of the 13th Modeling and Simulation Conf., Pittsburgh, April 1982, Vol. 13, Part 2 pp 645-654 (V.P.Srini, and J.F.Asenjo are the authors).

Architecture for Extended Abstract Dataflow, Proceedings of the 8th Annual Symposium on Computer Architecture, Minneapolis, May, 1981, pp 303-325.

A Reconfigurable Packet Switcher for Interconnecting Processors, Proceedings of IEEE Southeastcon, April, 1981, Huntsville, Alabama, pp. 225-231.

Abstract Dataflow Protocol for Communication in Distributed Computer Systems, Proceedings of COMPCON 1980, Washington, D.C., September, 1980, pp 321-332 (V.P.Srini, and B.D.Shriver are the authors).

Framework for Communication in Loosely Coupled Multiple Processor Systems, Proceedings of 1980 Parallel Processing Conference, Michigan, August, 1980, pp 49-52 (V.P.Srini, and B.D.Shriver are the authors).

Programming Language Specification by using Three Forms, Proc. of CSC Conf., Detroit, February, 1978.

The Class of Environment Operator Precedence Languages (EOPL'S), Proc. of CSC Conf., Atlanta, January, 1977.

Reports

AQUARIUS PROJECT - DARPA Semi-Annual Report, April. 1990 - Oct. 1990, DARPA contract No. N00014-88-K-0579.

AQUARIUS PROJECT - DARPA Semi-Annual Report, Nov. 1989 - March 1990, DARPA contract No. N00014-88-K-0579.

AQUARIUS PROJECT - DARPA Semi-Annual Report, April 1989 - Oct. 1989, DARPA contract No. N00014-88-K-0579.

Area Efficient Cells for LagerIV's DPP Library, Tech. Report No. UCB/CSD 89/531, Aug. 1989, Computer Science Div., Univ. of California, Berkeley, CA 94720.

The Aquarius-IIU Node: The caches, the Address Translation Unit, and the VME Interface, Tech. Report No. UCB/CSD 89/524, Aug. 1989, Computer Science Div., Univ. of California, Berkeley, CA 94720.

AQUARIUS PROJECT - DARPA Semi-Annual Report, Nov. 1988 - March 1989, DARPA contract No. N00014-88-K-0579.

The VLSI-PLM Board: Design, Construction, and Testing, Tech. Report No. UCB/CSD 89/499, Feb. 1989, Computer Science Div., Univ. of California, Berkeley, CA 94720. (L. Nguyen, L.G.Bushnell, V.P.Srini are the authors).

Multiprocessor Research for Prolog, Proc. of the State of California MICRO-1987 Project Reports, Feb. 1989 (V.P.Srini, A.M.Despain are the authors).

A computer Aided Design Methodology for Printed Circuit Boards, Tech. Report No. UCB/CSD 89/492, January 1989, Computer Science Div., Univ. of California, Berkeley, CA 94720. (L.G.Bushnell, V.P.Srini are the authors).

AQUARIUS PROJECT - DARPA Semi-Annual Report, May 1988 - Oct. 1988, DARPA contract No. N00014-88-K-0579.

Dynamically Reconfigurable Systems Research. NSF Final Report for Microelectronic System Architecture, DCR-8508344 and MCS-82-09400, August 1988. Also, Tech. Report No. UCB/CSD 88/441, August 1988, Computer Science Div., Univ. of California, Berkeley, CA 94720.

Designing and Implementing A CMOS Chip for Prolog DARPA Report for Task 6. Also, Tech. Report No. UCB/CSD 88/412 March 1988, Computer Science Div., Univ. of California, Berkeley, CA 94720.

Multiprocessor Architecture Research for Prolog, Proc. of the State of California MICRO-1986 Project Reports, Feb. 1988 (A.M.Despain, and V.P.Srini are the authors).

Comparative Performance Evaluation of the PLM and NCR 9300 System, Proceedings of the State of California MICRO-1985 Project Reports, March 1987 (A.M.Despain, V.P.Srini, and Y.N.Patt are the authors).

Architecture Research for Prolog Based on NCR/32, Proceedings of the State of California MICRO-1984 Project Reports, March 1986 (A.M.Despain, V.P.Srini, Y.N.Patt, and B.S.Fagin are the authors).

Iterative Network Model for RAM Chips, NCR Corp., Microprocessor Dept., Columbia, SC, 1975.

The Classes of Environment T-Operator Precedence Languages, Tennessee Tech. Univ., 1978.

Techniques for the Design, Specification, and Analysis of Languages for Microcomputer Systems, Tennessee Tech, Univ., 1978.

Other Papers

Instruction set Design for a Dataflow Processor, Jan. 1983.

DPL: A language for Distributed Systems, Rev. 1, Jan. 1983.

Predicting the Performability of Interconnection Networks, Dec. 1982.

Research Grants

USAF Grant: Low-power Parallel DSP Chip Design, Aug. 1994 to Oct. 1998.

DARPA Grant: Simulation System for the Wireless Communication of Multimedia Data, March. 1994 to Oct. 1994.

DARPA Grant: SBIR contract for "MCM Design for Methodology for Multitechnology Fabrication" Feb. 1992 to Aug. 1992.

NASA Grant: SBIR contract for "Parallel Implementation of Image Correspondence Algorithms for Rotorcraft" Feb. 1992 to Aug. 1992.

USAF Grant: SBIR contract for "Concurrent Engineering" May 1991 to Nov. 1991.

DARPA Grant: Research in System Architecture for the High Performance Execution of Logic Programs (A.M. Despain -P.I., and V.P. Srini - Project Director), July 1, 1988. Grant amount: \$880,000 per year.

NCR Corporation and MICRO: Multiprocessor Architecture Research for Prolog, July 1987 to June 1989, Univ. of California, Berkeley, CA 94720. Grant amount: \$200,000. (with Al Despain).

NCR Corporation and MICRO: Multiprocessor Architecture Research for Prolog, June 1986 to June 1987, Univ. of California, Berkeley, CA 94720. Grant amount: \$83,000. (with Profs. Al Despain and Yale Patt).

NCR Corporation and MICRO: Comparative Performance Evaluation of the PLM-TTL and NCR 9300 System, June 1985 to June 1986, Univ. of California, Berkeley, CA

94720. Grant amount: \$122,000. (with Profs. Al Despain and Yale Patt).

NCR Corporation and MICRO: Architecture Research for Prolog based on NCR/32 - 1-442427-54952, June 1984 to Dec. 1985, Univ. of California, Berkeley, CA 94720. Grant amount: \$104,045. (with Profs. Al Despain and Yale Patt).

National Science Foundation: Dynamically Reconfigurable Operating Systems Research - DCR-8508344, Aug. 15 1985 to April 30, 1987 and MCS-8209400, Feb. 1, 1983 to Sept 30, 1983. Grant amount: \$54,000.

Digital Equipment Corporation, Maynard, MA. Five LSI-11 systems to do research and teaching in interface design and operating system implementation at the University of Alabama in Birmingham, AL 35294. Grant amount: \$45,000.

Digital Equipment Corporation, Maynard, MA. Five GIGI color graphics systems to do research in graphical dataflow systems and VLSI design. Grant amount: \$25,000.

Texas Instruments, Inc., Corporate Engineering Center, Dallas, Texas: Grant D3151 (1979) to do research in Distributed Operating Systems at the University of Southwestern Louisiana, Lafayette, LA 70704, (Grant amount: \$300,000 Dr. B.D. Shriver and V.P. Srinini are the Co-PIs).

Research Reports (Data Flux Systems Inc.)

Low-Power Parallel DSP Chip for Multimedia data and 3-D Image Processing, Phase-II Final Report, Aug.. 1998 (submitted to U.S. Air Force, Eglin AFB, Florida).

Low-Power Parallel DSP Chip for Multimedia data and 3-D Image Processing, Phase-I Final Report, Oct. 1995 (submitted to U.S. Air Force, Eglin AFB, Florida).

Simulation Systems for the Wireless Communication of Multimedia Data, Nov. 1994 (submitted to Dept. of Defense, Advanced Research Project Agency).

Research Initiative in Multiple Digital Environments using Integrated Wireless and Wired Networks, Aug. 1994 (submitted to U.S. Army Research Office, NC).

Programmable Low-Power ATM Cell-Based Parallel DSP Chip for Speech, Vision, Sonar, and Video Processing, May 1994 (submitted to U.S. Navy).

Integrated Multimedia Capture, Storage, and Retrieval for Large Infrastructure Systems: An Approach and Some Challenges, April 1994 (submitted to Dept. of Defense, Advanced Research Project Agency).

Low-cost Multimedia Integrated Wireless System for the Visual Inspection of Aircraft, May 1994 (submitted to Dept. of Transportation, FAA)

Impact of Cognitive Rehearsal on Regaining Pilot Flight Proficiencies, April 1994 (submitted to Dept. of Transportation, FAA).

Programmable Realtime Full Screen and Full Motion Video Compression and Image

Processing Board for PCs, Dec. 1993 (submitted to Dept. of Defense, Advanced Research Projects Agency)

Integrated Multimedia Database for Breast Cancer Research, Dec. 1993 (submitted to National Cancer Institute).

Modeling and Simulating Integrated Wireless and Wired Network Systems for Multimedia Communication, Dec. 1993 (submitted to U.S. Navy).

Integrated Wireless and Wired Network Protocol Design and Implementation, Oct. 1993 (submitted to Dept. of Defense, TRP).

Software Architecture and Tools for Digital Library Servers, Oct. 1993 (submitted to Dept. of Defense, TRP).

Mobile Multimedia Communication Using Spread Spectrum Technology, July 1993 (submitted to U.S. Army).

Automated Multimedia Title Creation, July 1993 (submitted to Dept. of Defense, Advanced Research Project Agency).

Integrated Multimedia Data Capture, Storage, and Smart Retrieval in Command and Control Systems using Open Systems Architecture, July 1993 (submitted to U.S. Navy).

Computer-aided Generation of Hypermedia-based CD-ROM Titles, June 1993, (submitted to U.S. Navy)

Almost Realtime System Emulation Using an Array of FPGA Dies, June 1993 (submitted to U.S. Navy)

SARAM Based Digital Data Buffer for High Data Rates, June 1993 (submitted to U.S. Navy)

VLSI Based Digital MCM Design Methodology, Dec. 1992 (submitted to Dept. of Defense, DARPA).

Hardware and Software Architectures for Distributed Continuous Media (DCM) Services, Dec. 1992.

Computational Earth Systems Study based on Exchanges of Energy, Water, Heat, Carbon, and Trace Gases using Massively Parallel Computers, June 1992 (submitted to NASA).

Automated Concurrent Engineering in Computer and Communication Products, Dec. 1991 (submitted to U.S. Air Force).

Direct to Premise ACTS based Video Services: Experiments using T1-VSAT and the NASA Advanced Communications Technology Satellite (ACTS), Aug. 1991 (submitted to NASA).

Realtime Digital Image Capture, Storage, and Enhancement System for X-ray Video,

July 1991 (submitted to U.S. Army)

Single Module Multiprocessor System with Flexible I/O Bus Interface, June 1991
(submitted to Dept. of Energy).

Evaluating the Programmability of Dataflow Computer Systems, Dec. 1989 (submitted to
U.S. Air Force).

Theses and Books

Monograph: Architecture Analysis using Dataflow Graphs: Cray-1S as Case Study, CS
Dept., University of Alabama in Birmingham, University Station, AL 35294. Second
author on the work is Jorge F. Asenjo.

Dissertation: An Extended Abstract Dataflow Methodology for Designing and Modeling
Reconfigurable Systems, CS Dept., University of Southwestern Louisiana, Lafayette, LA
70504, July, 1980.

Mechanisms for Specifying and Analyzing Extensible Languages, CS Dept., VPI&SU,
Blacksburg, VA 24061, 1977.

M.S. Thesis: Simulated Analysis of Digital and Nonlinear Circuits using the Continuous
System Modeling Program (IBM S/360 CSMP), EE Dept., Tennessee Tech. Univ., 1971.

B.E. Project Works: (1) Component Design of Digital Computers. (2) Unbalanced
Operation of Induction Motors, EE Dept., College of Engineering, Guindy, Madras-25,
1969.

Tutorials

Multiprocessor Design Using VLSI Components, (two days) University of California,
Berkeley, March 1991, June 1990, and Third Intl. Workshop on VLSI Design, Bangalore,
India, Jan. 1990.

VLSI Processor Design Using Semicustom Methodology, (two days) University of
California, Berkeley, Sept. 1989, and Second Intl. Workshop on VLSI Design,
Bangalore, India, Dec. 1988.

Logic Programming, (one day) 19th Hawaii Intl. Conf. on System Sciences, Honolulu,
Jan. 1986.

Dataflow Computers: Architecture and Programming, (three days)

National University of Taiwan, Taipei, Republic of China, March 1983.

Dataflow methodology for Distributed Operating System Design, (one day) Texas
Instruments Inc., Houston, TX, March 1981.

Dataflow Architecture, (one day) Hewlett-Packard, Corporate Research Labs, Palo Alto,
CA, July 1980.

Invited Talks and Short-courses

Deep submicron Flows for Single Chip CMOS Radios to do Multimedia Communication, Mentor Graphics Corp., Wilsonville, OR, Jan., 2000

Multimedia Enabled Pocket Computer Research for the Next Decade, Series of talks at Fujitsu Lab. for three days, Kawasaki, Japan, July 1998

Web Browser Design and API Generation Research, Series of talks at Fujitsu Lab. for three days, Kawasaki, Japan, 1995

Full-Speed Emulation of High Performance Microprocessors, Intel Corp. and QuickTurn Systems, Aug. 1993.

Hardware and Software Architectures for Continuous Media, Fujitsu Lab., Japan, Jan. 1993.

VLSI Based MCM Design Methodology and Automated Concurrent Engg., Fujitsu Lab., Japan, Jan. 1993.

Fast Superscalar Processor Design and Implementation, Fujitsu Lab., Japan, Jan. 1993.

VHDL for Designing and Modeling ASIC Based Systems, Fujitsu, Japan, April 1991.

Challenges in Parallel System Design and Implementation, Fujitsu, Japan, April 1991.

Programming for Parallelism, Fujitsu, Japan, April 1991.

Parallel Algorithms, Models, Languages, and Compilers, Fujitsu, Japan, April 1991.

Framework for Proof of Concepts, Fujitsu, Japan, April 1991.

Parallel Processing PC using Xbar-Multi, Talk at Apple Computers, May 1989.

2D-BUS Multiprocessor System, Talk at SRI, OSU, and UCSC, Nov. 1988

Analysis of Cray-1S Architecture, T.J.Watson Research Center, IBM, Yorktown Heights, June 1983.

NCR32000 and its use in a Dataflow Processor, NCR Corp., Computer Division, San Diego, CA, Feb. 1983.

Dataflow Architecture and Processor Design, Digital Equipment Corp., Maynard, MA, July 1981, Hudson, July 1982.

Dataflow Processors, Univ. of Mass., Amherst, Feb. 83.

An architecture for extended abstract dataflow, NASA Ames, Computational Fluid Dynamics Group, Moffett Field, CA, Sept. 1981.

Dataflow Methodology for Reconfigurable System Design, Bell Labs, Holmdale, NJ,

June 1980.

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